



## **RFLM-102202XA-150**

### **Quasi Active High Power L Band PIN Diode Limiter Module - SMT**

#### **Features:**

- Surface Mount L- Band Limiter Module: 9mm x 6mm x 2.5mm
- Frequency Range: 1 to 2 GHz
- High Average Power Handling: +57 dBm
- High Peak Power Handling: +60 dBm
- Low Insertion Loss: < 0.7 dB
- Return Loss: >13 dB
- Flat Leakage Power : <20 dBm
- Spike Energy Leakage: <0.5 ergs
- No external control lines or power supply required
- RoHS Compliant

#### **Description:**

The RFLM-102202XA-150 SMT Silicon PIN Diode Limiter Module offers protection against 450W CW High Power CW and 1kW Peak protection in the L-Band region. It is based on proven hybrid assembly technique utilized extensively in high reliability, mission critical applications for several decades. The RFLM102202XA-150 offers excellent thermal characteristics in a compact, low profile 9mm x 6mm x 2.5mm package. The RFLM-102202XA-150 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the L Band frequency range.

The limiter RF circuit characteristics provide outstanding passive (always on) receiver protection against High Average Power up to +57 dBm, and High Peak Power up to +60 dBm pulsed while maintaining low flat leakage to less than 20 dBm, and reduces Spike Leakage to less than 0.5 ergs.

#### **ESD and Moisture Sensitivity Rating**

The RFLM102202XA-150 Limiter Module carries a Class 0 ESD rating (HBM) and an MSL 1 moisture rating.

#### **Thermal Management Features**

The RFLM-102202XA-150 based substrate has been designed to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. The multi-stage limiter design employs an ultra-fast detection circuit which accelerates the turn on period of the coarse stage and a proprietary clean up stage which minimizes the leakage of the limiter. The proprietary multi-stage limiter

design also minimizes the thermal resistance from the High Power handling coarse stage to base plate ( $R_{THJA}$ ). This circuit topology coupled with the thermal characteristic of the substrate design enables the limiter to reliably handle High Input RF Power up to +57 dBm CW and RF Peak Power levels up to +60 dBm (25 uSec pulse width @ 1% duty cycle with base plate temperature at +85°C).

## Absolute Maximum Ratings

@  $Z_0=50\Omega$ ,  $T_A=+25^\circ\text{C}$  as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	$T_{CASE}=+85^\circ\text{C}$ , source and load VSWR < 1.2, RF Pulse width = 25 usec, duty cycle = 1%, derated linearly to 0 W at $T_{CASE}=+150^\circ\text{C}$ (See note 1)	+60 dBm
RF CW Incident Power		+57 dBm

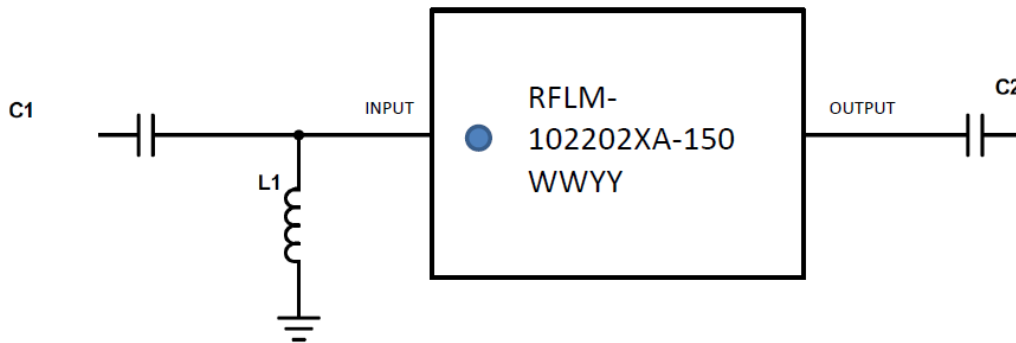
Note 1:  $T_{CASE}$  is defined as the temperature of the bottom ground surface of the device.

## RFLM102202XA-150 Electrical Specifications

@  $Z_0=50\Omega$ ,  $T_A=+25^\circ\text{C}$  as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	1 GHz $\leq$ F $\leq$ 2 GHz	1		2	GHz
Insertion Loss	IL	1 GHz $\leq$ F $\leq$ 2 GHz, $P_{in}=0$ dBm		0.5	0.7	dB
Insertion Loss Rate of Change vs Operating Temperature	$\Delta$ IL	1 GHz $\leq$ F $\leq$ 2 GHz, $P_{in} \leq -10$ dBm		0.005		dB/°C
Return Loss	RL	1 GHz $\leq$ F $\leq$ 2 GHz, $P_{in}=0$ dBm	13	15		dB
Input 1 dB Compression Point	$IP_{1dB}$	1 GHz $\leq$ F $\leq$ 2 GHz	8	10	12	dBm
2 <sup>nd</sup> Harmonic	$2F_o$	$P_{in}=0$ dBm, $F_o=2.0$ GHz		-50	-45	dBc
Peak Incident Power	$P_{inc(PK)}$	RF Pulse = 25 usec, duty cycle = 1%, $t_{rise} \leq 2$ us, $t_{fall} \leq 2$ usec			60	dBm
CW Incident Power	$P_{inc(CW)}$	1 GHz $\leq$ F $\leq$ 2 GHz			57	dBm
Flat Leakage	FL	RF Pulse width = 25 us, duty cycle = 1%, $t_{rise} \leq 2$ us, $t_{fall} \leq 2$ us			20	dBm
Spike Leakage	SL	RF Pulse width = 25 us, duty cycle = 1%		0.5	0.6	erg
Recovery Time	$T_R$	50% falling edge of RF Pulse to 1 dB IL, $P_{in} = 50$ dBm peak, RF PW = 25 us, duty cycle = 1%, $t_{rise} \leq 2$ us, $t_{fall} \leq 1$ usec		1	2	usec

### RFLM-102202XA-150 Schematic with Off Board Components

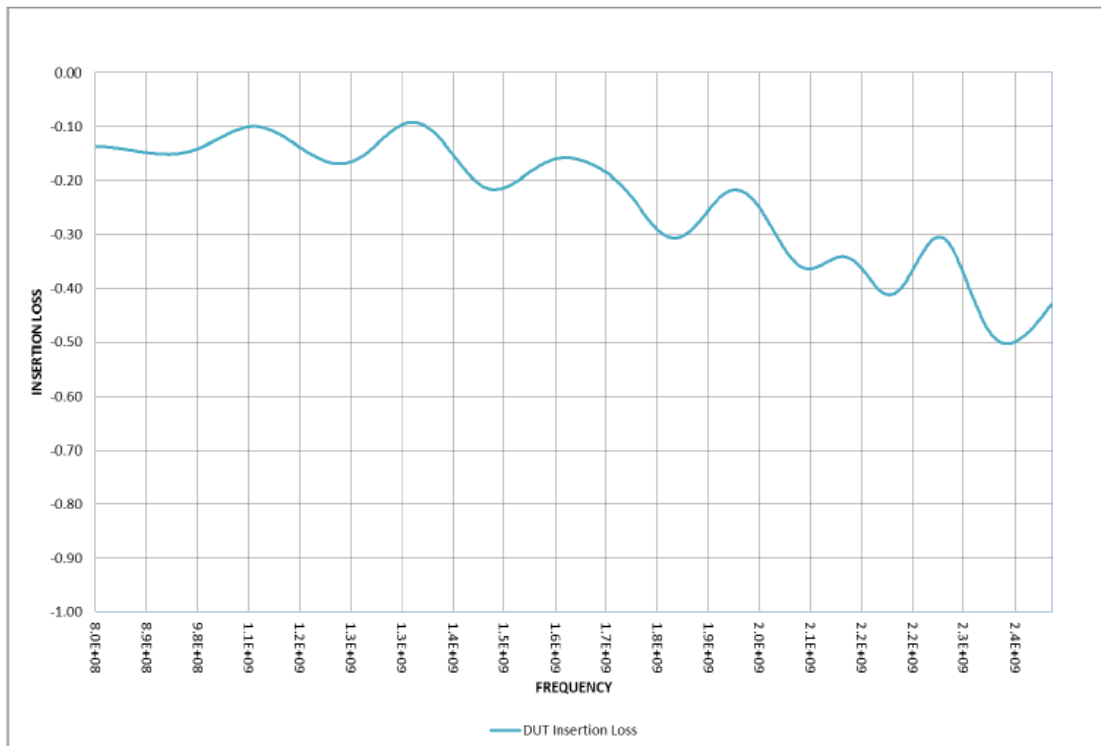


The RFLM-102202XA-150 requires an external input and output coupling capacitors (C1 & C2) as well as a tuning inductor (L1) connected to the input port of the limiter module.

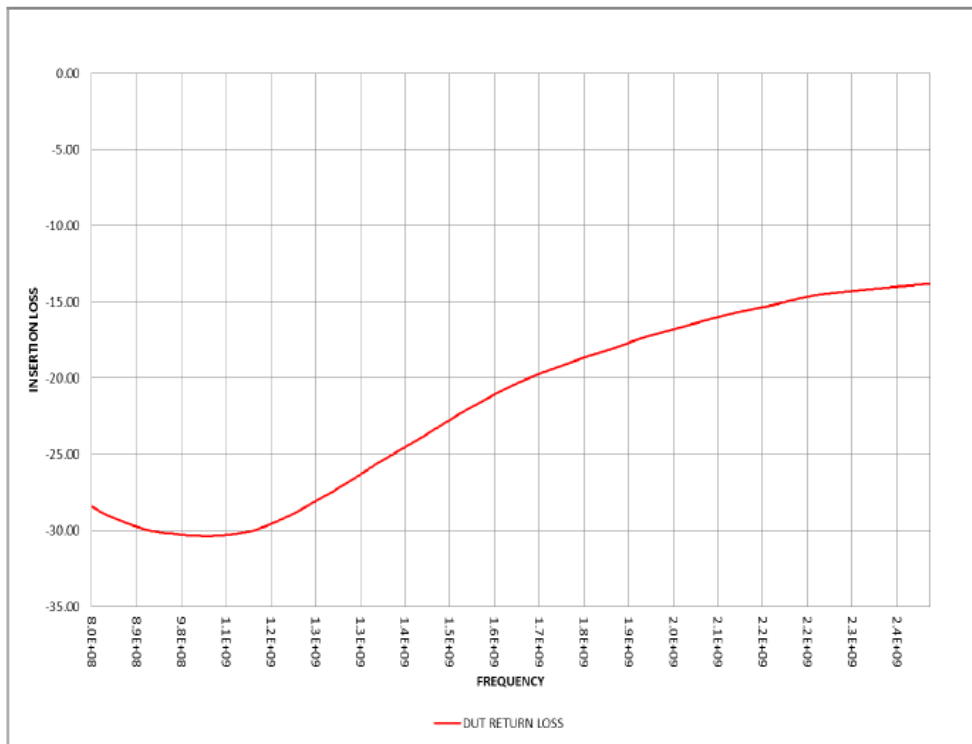
### RFLM-102202XA-150 Typical Performance

$Z_o = 50\Omega$ ,  $T_{CASE} = 25^\circ C$ ,  $PIN = -20\text{ dBm}$  as measured on the Ground Plane of the device.

RFLM-102202XA-150 Insertion Loss vs Frequency - TARGET



RFLM-102202XA-150 Return Loss vs Frequency - TARGET

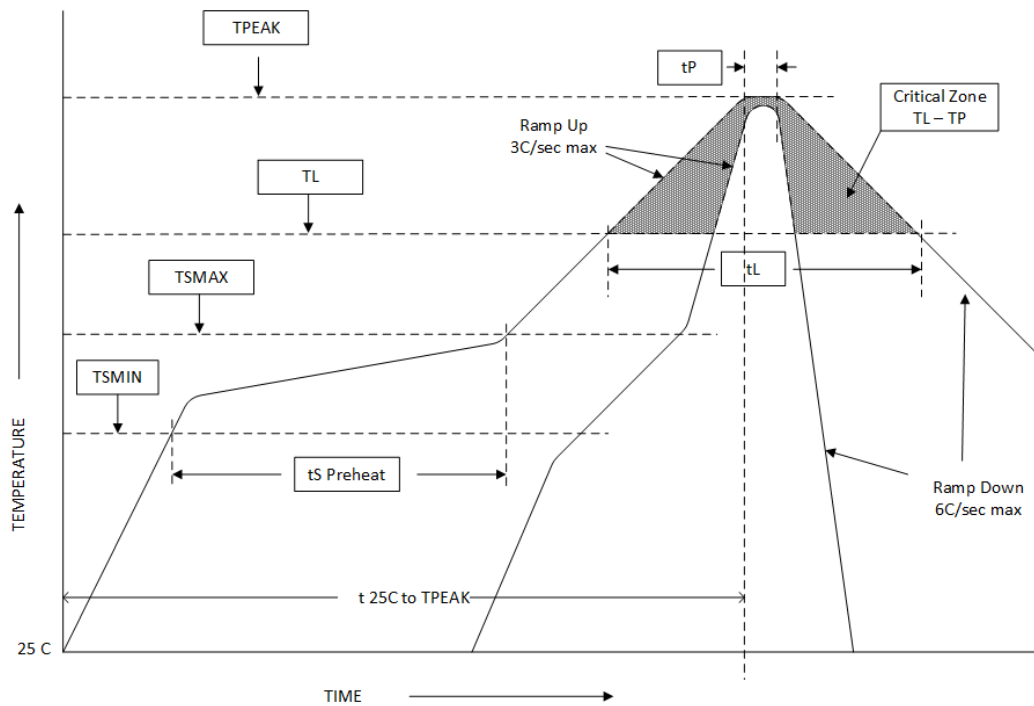


Assembly Instructions

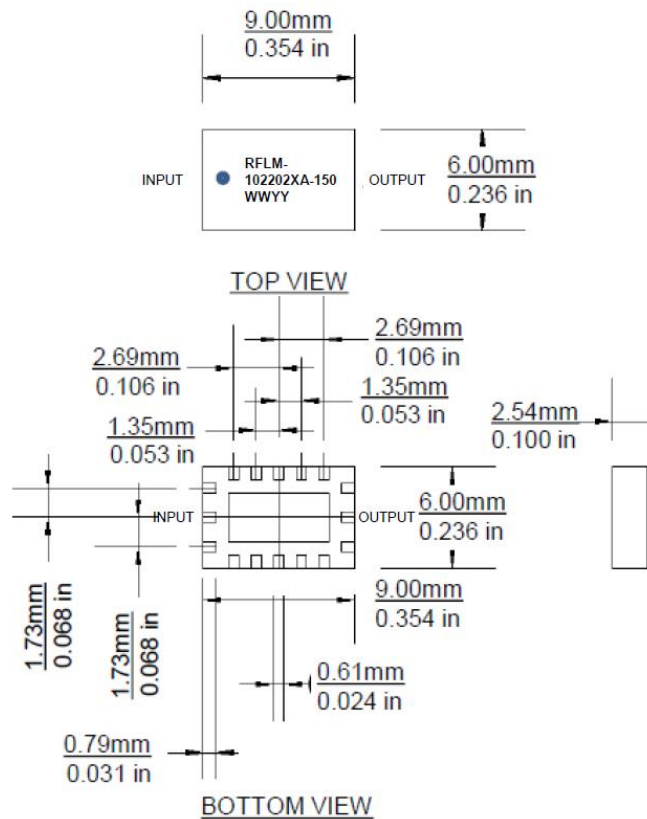
The RFLM-102202XA-150 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/sec (max)	3°C/sec (max)
Preheat		
Temp Min ( $T_{smin}$ )	100°C	100°C
Temp Max ( $T_{smax}$ )	150°C	150°C
Time (min to max) ( $t_s$ )	60 – 120 sec	60 – 120 sec
$T_{smax}$ to $T_L$		
Ramp up Rate		3°C/sec (max)
Peak Temp ( $T_P$ )	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp ( $T_P$ )	10 to 30 sec	20 to 40 sec
Time Maintained Above:		
Temp ( $T_L$ )	183°C	217°C
Time ( $t_L$ )	60 to 150 sec	60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to $T_P$	6 minutes (max)	8 minutes (max)

### Solder Re-Flow Time-Temperature Profile



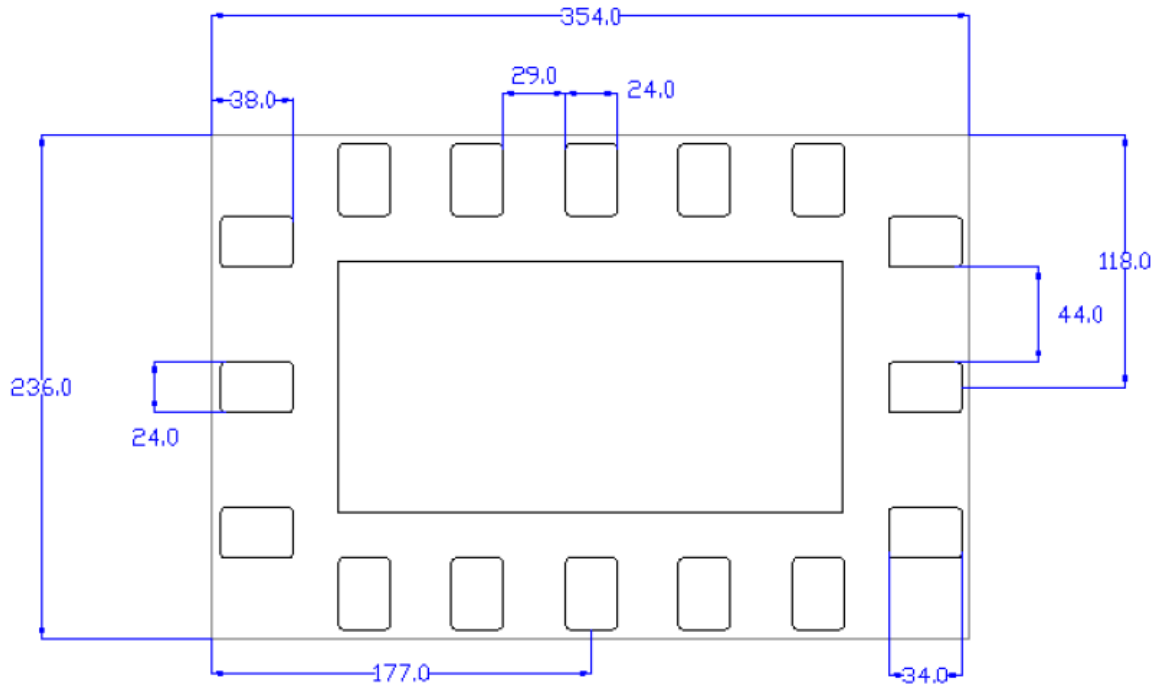
### RFLM-102202XA-150 Limiter Module Package Outline Drawing



Notes:

- 1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
- 2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).

**Recommended RF Circuit Solder Footprint for the RFLM102202XA-150**



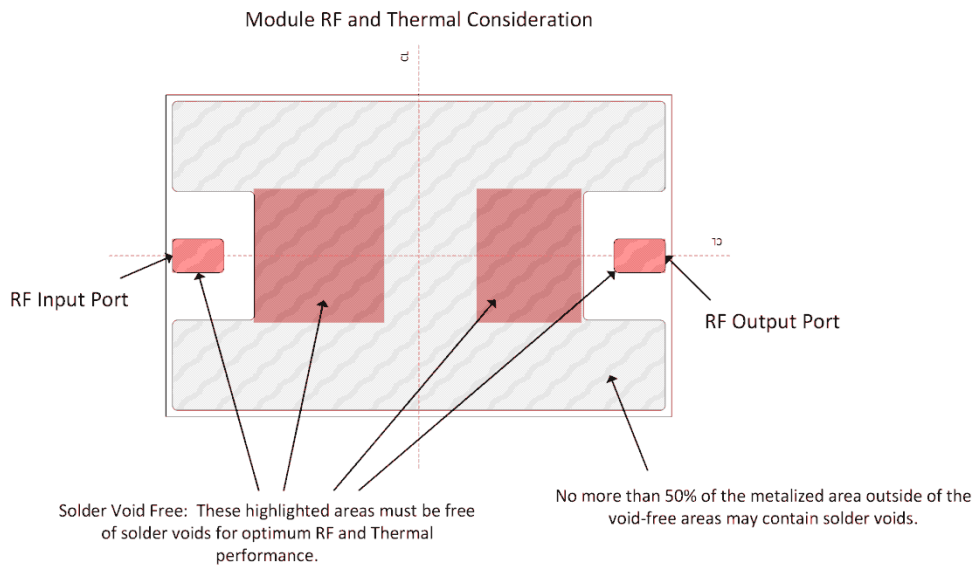
Notes:

- 1) Recommended PCB material is Rogers 4350B, 10 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
- 2) Center Ground Plane area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.

## Thermal Design Considerations:

The design of the RFLM-102202XA-150 family of Limiter Modules permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 85°C.

There must be a minimal thermal and electrical resistance between the limiter bottom surface and ground. Adequate thermal management is required to maintain a  $T_{JC}$  at less than +175°C and thereby avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the area shaded in red in the figure shown below:



## Part Number Ordering Detail:

The RFLM-102202XA-150 Limiter Module is available in the following formats:

Part Number	Description	Packaging
RFLM-102202XA-150	L-Band Limiter, No DC Blocking Caps	Gel-Pack