PRELIMINARY

RFuW Engineering Pte. Ltd.

RFLM-502602HC-491

High Power C Band Limiter Module: Ultra Low Flat Leakage & Fast Recovery Time

Features:

- Frequency Range: 5.0 to 6.0 GHz
- High Peak Power Handling: +57 dBm
- High Average Power Handling: +50 dBm
- Insertion Loss: <0.8 dB
- Return Loss: >15 dB
- Flat Leakage Power: <14 dBm
- Spike Energy Leakage: <0.5 ergs
- Recovery Time: <200 nsec
- SMT Limiter Module : 9mm x 6mm x 2.5mm
- DC Blocking Capacitors
- "Always On Protection"
    - - No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-502602HC-491 SMT Silicon PIN Diode Limiter Module offers "Always On" High Power CW and Peak protection in the C-Band region. This Limiter Modules are based on proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-502602HC-491 offers excellent thermal characteristics in a compact, low profile 6mm x 9mm x 2.5mm package. They designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the C Band frequency range.

The RFLM-502602HC-491 Limiter Module provides outstanding passive receiver protection (Always on) which protects against High Average Power up to +48 dBm @ Tcase=+85^{o}C, High Peak Power up to +57 dBm (Peak) Pulse Width = 25 usec, Pulse Repetition Rate = 5%, Tcase=+85^{o}C, maintains low flat leakage to less than 14 dBm (typ), and reduces Spike Leakage to less than 0.5 ergs(typ).

ESD and Moisture Sensitivity Rating

The RFLM-502602HC-491 Limiter Module carries a Class 1C ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The proprietary design methodology minimizes the thermal resistance from the PIN Diode junction to base plate (R_{THJ}-A) to less than 25°C/W. The two stage limiter design employs a two stage detector circuit which enables ultra-fast turn on of the High Power PIN Diodes. This circuit topology coupled with the thermal characteristic of the substrate design enables the Limiter Module to reliably handling High Input RF Power up to +48 dBm CW and RF Peak Power levels up to +57 dBm (25 uSec pulse width @ 5.0% duty cycle) with base plate temperature at +85°C.The RFLM-502602HC-491 based substrate has been design to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns.

Absolute Maximum Ratings

@ Z_0=50Ω, T_A= +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=85°C, source and load VSWR < 1.2:1, RF Pulse width = 25 usec, duty cycle = 5%, derated linearly to 0 W at T_{CASE}=150°C (note 1)	+57 dBm
RF CW Incident Power	T_{CASE}=+85°C, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE}=150°C (note 1)	+48 dBm
RF CW Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE}=150°C (note 1)	+50 dBm
θ_{JC} Thermal Resistance	From Diode Junction to bottom surface of package	25°C/W
RF Input & Output DC Block Capacitor Voltage Breakdown		100 V DC

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

RFLM-2062352HC-491 Electrical Specifications

@ Z_o=50Ω, TA= +25°C as measured on the base ground surface of the device.

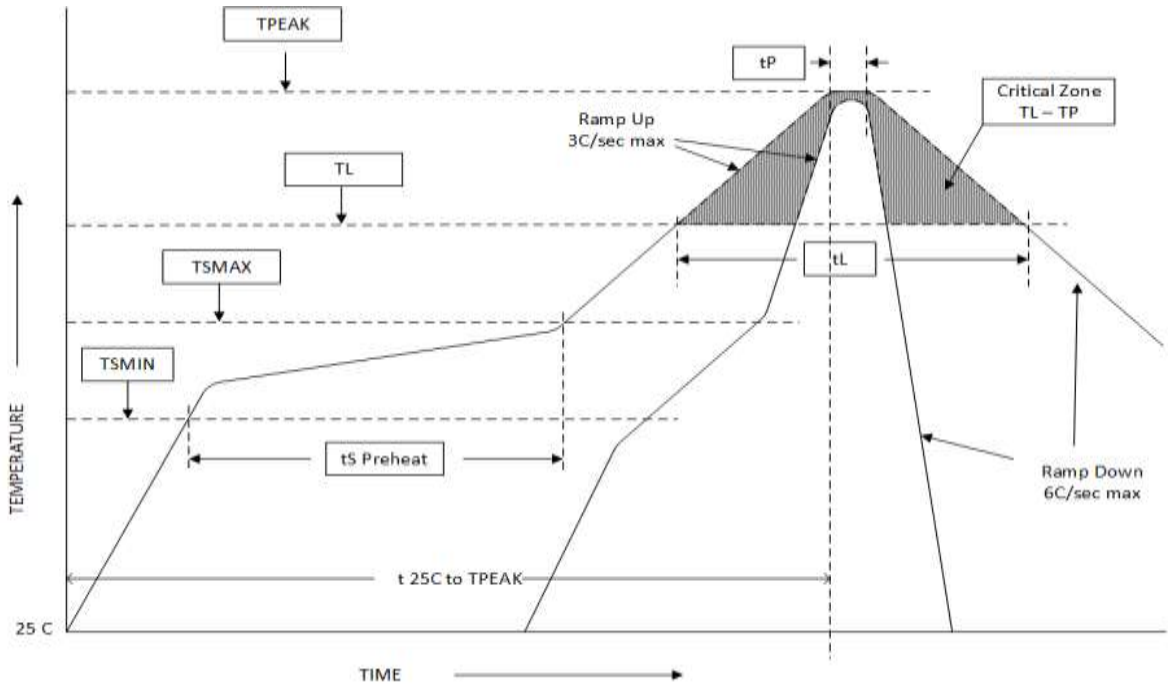
Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	5.0 GHz ≤ F ≤ 6.0 GHz	5.0		6.0	GHz
Insertion Loss	IL	5.0 GHz ≤ F ≤ 6.0 GHz, P_{in}= -10dBm		0.65	0.8	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	5.0 GHz ≤ F ≤ 6.0 GHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	5.0 GHz ≤ F ≤ 6.0 GHz, Pin= -10dBm	15	17		dB
Input 1 dB Compression Point	IP_{1dB}	5.0 GHz ≤ F ≤ 6.0 GHz	0	9	10	dBm
2nd Harmonic	$2F_o$	P_{in}= -10 dBm, F_o= 3.0 GHz		-40	-30	dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 25 usec, duty cycle = 5%, t_{rise} ≤ 3us, t_{fall} ≤ 3usec			+57	dBm
CW Incident Power	$P_{inc(CW)}$	5.0 GHz ≤ F ≤ 6.0 GHz T_{case} = +85°C			+48	dBm
Flat Leakage	FL	P_{in} = +57 dBm, RF Pulse width = 25 us, duty cycle = 5%, t_{rise}≤ 3 us, t_{fall}≤ 3 us			14	dBm
Spike Leakage	SL	Pin = +57 dBm, RF Pulse width = 25 us, duty cycle = 5%			0.5	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = +57 dBm peak, RF PW = 25 us, duty cycle = 5%, trise ≤ 3us, t_{fall} ≤ 3usec		100	200	nsec

Assembly Instructions

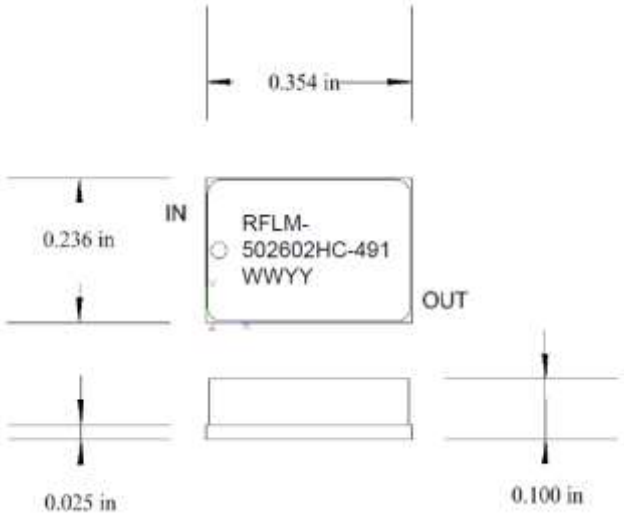
The RFLM-502602HC-491may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

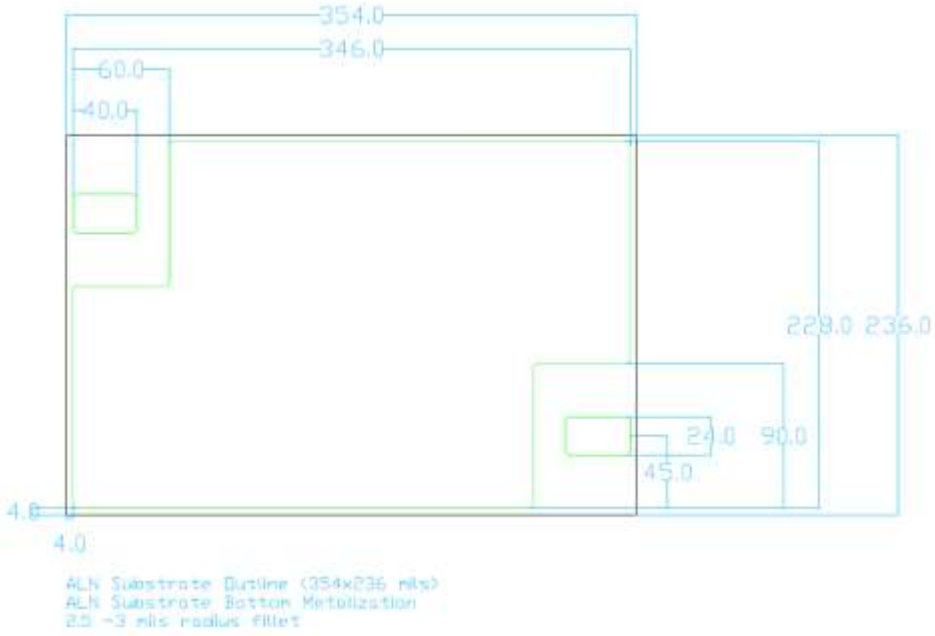
Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 180 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFLM-502602HC-491 Limiter Module Package Outline Drawing





Notes:

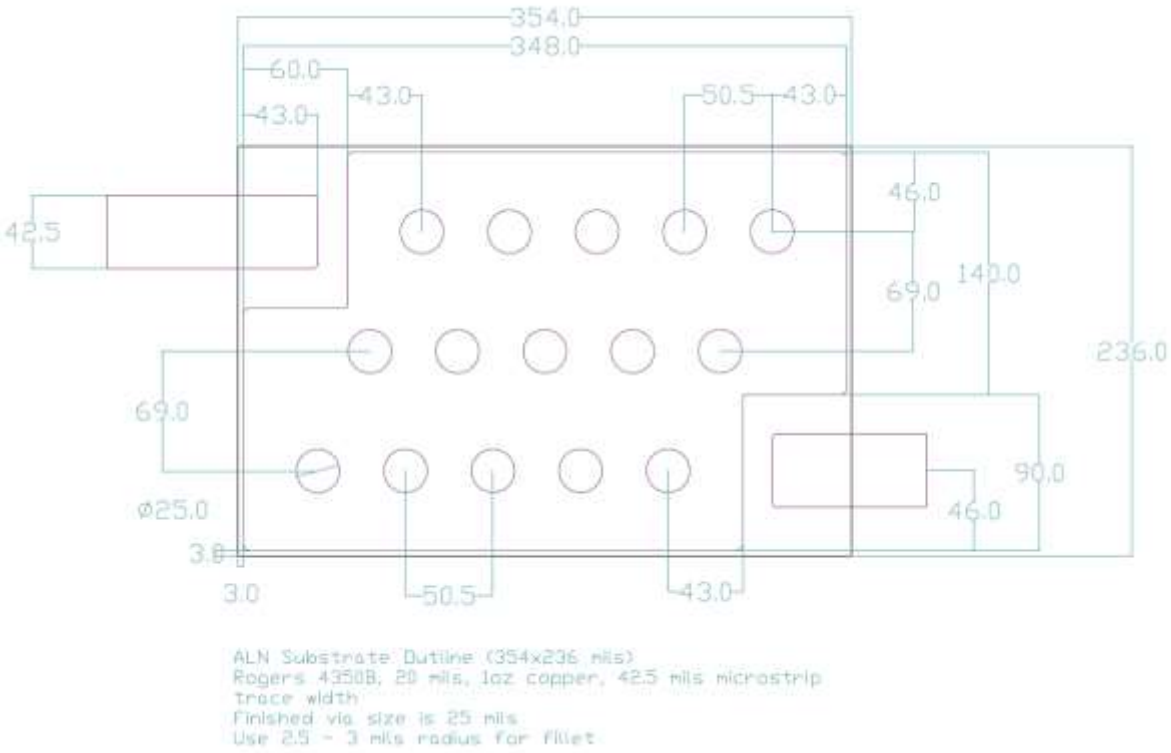
1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).
3) Unit = mils

Thermal Design Considerations:

The design of the RFLM-502602HC-491Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 85°C.

There must be a minimal thermal and electrical resistance between the limiter module and ground. Adequate thermal management is required to maintain a Tjc at less than +175°C and thereby avoid adversely affectingthe semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.

Recommended RF Circuit Solder Footprint for the RFLM-502602HC-491



Notes:

1) Recommended PCB material is Rogers 4350B, 20 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.
3) Unit = mils

Part Number Ordering Detail:

The RFLM-502602HC-491 Limiter Module is available in either tube or Tape & Reel format.

Part Number	Description	Packaging
RFLM-502602HC-491	C Band Limiter with Input & Output DC Blocking Caps	Gel Pack